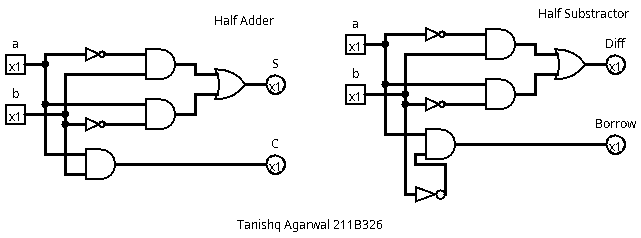
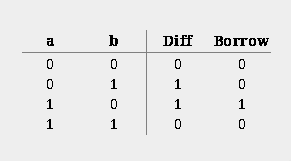
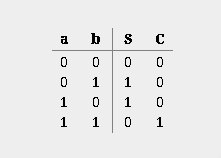
**EXPERIMENT#2**

**Aim: Design of binary adders and subtractors.**

**Exercise#1:** Design half adder and half subtractor shown in Fig. 1 and Fig. 2 using logisim simulator.

**Logic Diagram :**

**Boolean expression and Truth Table :**

S: ~a b + a ~b

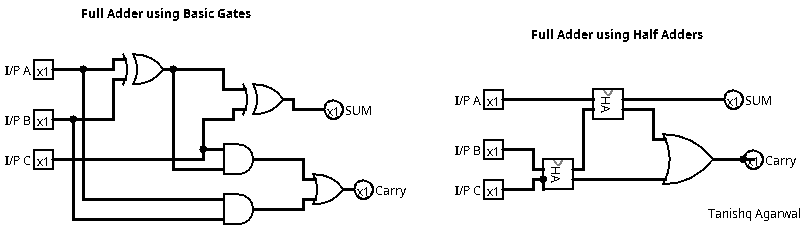
C: a b

Diff: ~a b + a ~b

Borrow: a ~b

**Exercise#2:** Design full adder using (i) basic gates only (ii) by adding half adder as sub circuit using logisim.

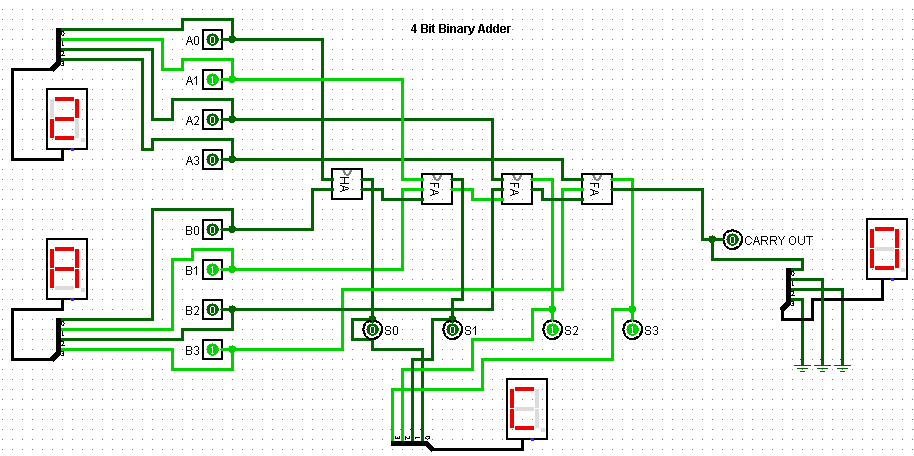
**Logic Diagram :**

****

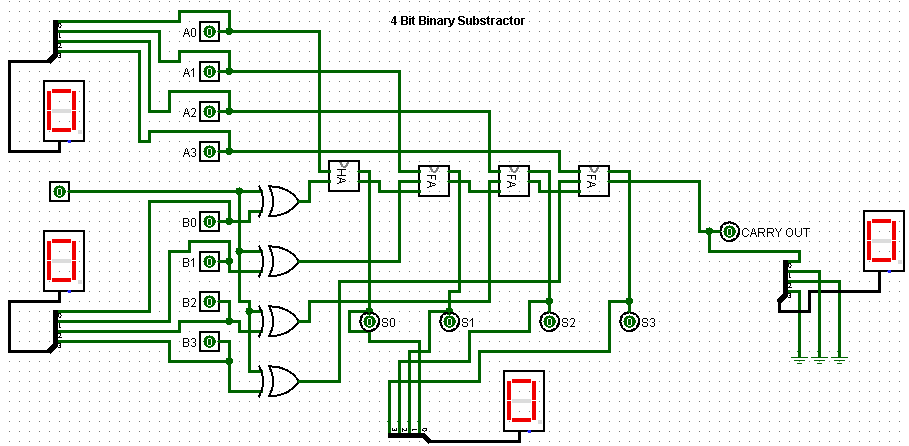
**Boolean expressions and K-Maps :**

|  |  |
| --- | --- |
| **Sum** | **Carry** |
|  |  |

**Exercise#3:** Design 4-bit binary adder using one half adder and 3-full adders as shown in Fig. 5. Use half adder and full adders as sub circuits in the design. Display both the input digits; output digit and end carry digit using Hex digit display with splitter available in logisim simulator.

**Logic Diagram:**

**Exercise#4:** Design 4-bit binary adder-subtractor using full adders as shown in Fig. 6. Use full adders as sub-circuits in the design. Display both the input digits, initial carry digit; output digit, and end carry digit usingHex digit display with splitter available in logisim simulator.

**Logic Diagram:**